ABSTRACT OF THE DISCLOSURE

A semiconductor memory device capable of accurately simulating a read-out timing of a memory cell and enhancing a production yield is provided. A dummy column selector is placed so as to be connected to dummy bit lines, and a plurality of dummy cells driving the dummy bit lines are placed at positions farthest in a column direction on a memory array from the side where an amplifier circuit is placed. This configuration allows a timing for driving the bit lines by the memory cells that are placed similarly at positions farthest from the amplifier circuit to be simulated accurately, thus enabling the generation of an amplifier startup signal without delay. Furthermore, a plurality of dummy word lines respectively connected to the plurality of dummy columns allow for readily switching from a dummy cell with a defect to a normal dummy cell.